Introduction

- Network Processors are currently of great interest to many companies (Intel, IBM etc.)
- They integrate the best features of custom ASICs and general purpose processors
- The Intel IXP1200 was one of the first Network Processors available in the market.
- This project revolves around measuring the performance of the IXP1200.

IXP1200 Architecture

- StrongArm core processor with 6 programmable RISC based microengines
- StrongArm core is used for control plane functionality (routing table maintenance etc.) while microengines handle data plane functionality (packet classification, packet I/O etc.)
- Scratchpad RAM / SRAM / SDRAM
- Standard 32bit PCI bus and fast 64bit IX bus controlled by FBI unit

Microengines

- 6 microengines
- Single pipelined in-order RISC processor with customized instruction set optimized for packet processing
- Each microengine can run 4 separate threads with a different PC for each thread and hardware assisted super-fast context switching
- 256 registers per microengine
- 128 32bit general purpose registers
- 128 32bit transfer registers to access SDRAM and SRAM
- 32 bit ALU and shifter

Architecture

IPC / Instructions in Flight

- Both graphs look similar as the microengines do not do any form of out-of-order speculation. Hence the maximum IPC value is 1 and the maximum number of instructions in flight is 5
Branch Predictions

- Microengines have 3 mechanisms to improve branch predictions
  - Deferred Branches
  - Setting Condition code earlier
  - Branch guessing with programmer assistance

- From graphs, different applications can have totally different branch prediction results. It depends a lot on the programmer.

Memory Access Latencies

- Memory Access Latencies are big (> 50% of accesses to SDRAM take at least 75 cycles for example)

- Latency is hidden by multiple threads on each microengine. When 1 thread is I/O bound, another thread can do useful work on the microengine.